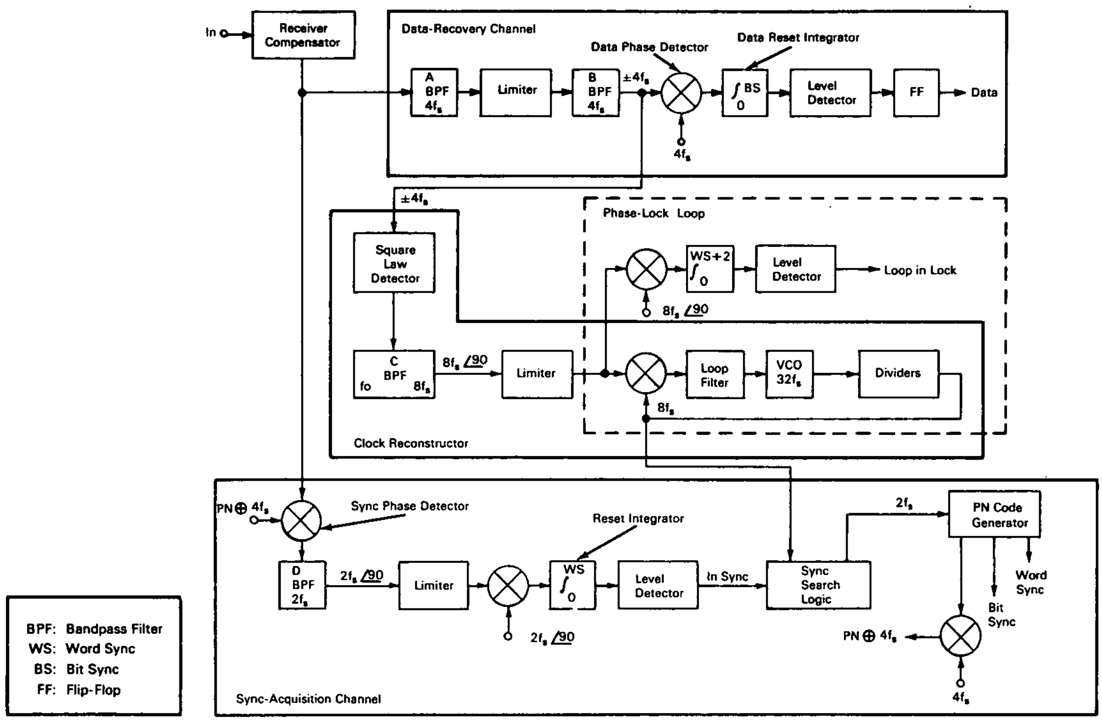
NASA TECH BRIEF

PN Acquisition Demodulator Achieves Automatic Synchronization of a Telemetry Channel



The problem:

To provide an automatic means for obtaining initial word and bit synchronization in a pulse-code-modulated/phase-shift-keyed digital communications system. One solution has been to continuously transmit synchronism information over the channel, in parallel with the data information in the form of a pseudorandom (pseudonoise, PN) sequence with a two-level autocorrelation function. The most difficult problem in such a system is the detection of the maximum in the cross correlation between the noisy and the replica codes during initial synchronization. Present methods often require extensive manual operations which are generally time consuming and inefficient.

The solution:

A data demodulator for automatic sync acquisition. Basically, the system generates a clock frequency harmonically related to the PN code generator clock but of ambiguous phase, and then solves the ambiguity by digitally retarding or advancing the ambiguous clock phase until the maximum in the cross-correlation is detected, The ambiguous clock is easily generated

(continued overleaf)

in the two-subcarrier (double-channel) system by utilizing a quadratic detector to remove the data modulation from the 180° phase-shift-keyed subcarrier.

How it's done:

The composite input signal to the demodulator is made up of a synchronization PN code multiplying a $2f_s$ subcarrier which is linearly added to data multiplying a $4f_s$ subcarrier. The PN code is clocked at $2f_s$. This signal is described in the equation:

$$\text{Sig In} = PN \oplus 2f_s + 4f_s \oplus \text{Data}.$$

The input signal is applied to bandpass filter (BPF) A and a synchronization phase detector. Bandpass filter A passes only the $4f_s$ subcarrier and data which are amplified, limited, and refiltered by a limiter amplifier and bandpass filter B. The output of bandpass filter B is applied to a data phase detector and a square law detector. The output of the data phase detector is applied to the data reset integrator which is reset by the bit-sync signal obtained by decoding a specific state of the local PN generator. The polarity at the end of each integration is detected and utilized to steer a flip-flop, the output of which is data. The square law detector eliminates data from the signal at its input. The output of the square law detector passes through bandpass filter C which is centered at $8f_s$. The resulting $8f_s$ sine wave is limited and applied to a phase-lock loop. The voltage controlled oscillator (VCO) in this loop serves as the clock source for all digital signals generated in the demodulator. Included in these digital signals are PN, $PN \oplus 4f_s$, $8f_s$, $8f_s\underline{/90°}$, $4f_s$, $2f_s$, $2f_s\underline{/90°}$ and the word- and bit-sync signals.

In the synchronization phase detector, the incoming signal is multiplied by local $PN \oplus 4f_s$ which results in $2f_s\underline{/90°}$ (when the incoming and local PN codes are aligned). This $2f_s\underline{/90°}$ is filtered, limited, and multiplied by local $2f_s\underline{/90°}$. The output of this last multiplier is applied to a reset integrator which is reset at word-sync intervals. This integrator is biased so that a positive output exists only at the maximum in the cross-correlation between the received local and the PN codes. The output of the reset integrator is applied to a level detector circuit, which in turn steers a flip-flop which yields an in-sync signal when the integrator output is positive.

Notes:

Inquiries concerning this invention may be directed to:

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Reference: B66-10271

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C., 20546.

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